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Modified SeriesConnected Multilevel Inverter

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***Abstract*—This study presents a particular design for staggered inverter that work in symmetric way. The proposed secluded staggered inverter can create flight of stairs yield voltage waveform that incorporates all voltage levels. The proposed staggered inverter is contrasted and regular flowed staggered inverter regarding number of switches. Multicarrier sinusoidal heartbeat width balance conspires took on for producing exchanging signals. The viability of proposed particular staggered inverter is confirmed through reproduction and exploratory execution.**

Keywords—Cascaded Multilevel inverter; less number of devices; sinusoidal pulse width modulation; total harmonic distortion

I. INTRODUCTION

Multilevel inverters (MLI) have achieved increasing acceptance in high and medium power applications. Recently, for high power application, multilevel converters are widely used such as static var compensators, electric drives, active power filters and renewable energies application. The advantages of MLI are high quality output waveform, less harmonic distortion and better electromagnetic capability [1]–[6]. However, MLI have some demerits, that is, required number of power semiconductor switches along with circuit components such as gate driver circuit, protection circuit. This makes intricacy in circuit, more installation area, expensive and reduces the efficiency & reliability of the inverter. Generally, MLIs are classified in three topology as neutral point clamped (NPC), flying capacitor (FC) and cascaded H-bridge (CHB) [1]–[9]. Among the conventional topologies, CHB has received wide response because of its modular structure. However, CHB MLI required isolated dc voltage source is a limitation of the topology [7]. A CHB is classified in to two categories as symmetric and asymmetric MLI on the basis of magnitude DC voltage source. In symmetric MLI, the magnitudes of DC sources are equal, whereas in asymmetric MLI magnitudes of DC sources are unequal. Asymmetric MLI reduced the installation area and cost of inverter circuit. The asymmetric CHB MLI generates higher number of voltage step as compared to symmetric MLI with equal number of power semiconductor switches [7] but switching scheme is complex and there is possibility to lose the modularity. A modular structure for symmetric MLI with less number of switches is addressed in this paper.

II. PROPOSED MULTILEVEL INVERTER

The modular structure (basic module) for proposed MLI is shown in Fig. 1. This basic module consists of two isolated dc sources and six power electronics switches. As seen from this structure, to avoid the short circuit, the lower and upper corresponding switches should not be turned on simultaneously. So switches Sn1', Sn2' and Sn3' are operate in complementary fasion with Sn1, Sn2 and Sn3, respectively. The magnitude of isolated dc sources is same forbasicmoduleof proposed multilevel inverter.

Each module can produce five voltage levels that include all voltage levels (zero, positive and negative) in symmetric schemeas shown in Fig. 2. Therefore,this configuration does not required H-bridge OR any additional circuit to generates negative voltage levels.

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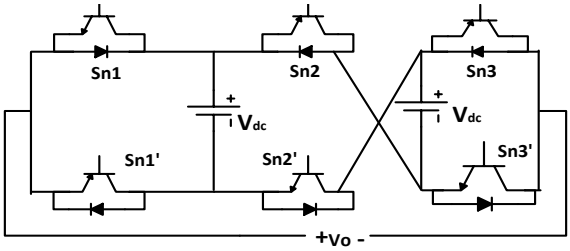

Fig. 1*Basic module of proposed MLI*

TABLE I LOOK-UP TABLE SWITCHING STATE FOR BASIC MODULE

S.no.	***Level of combined Signal***	***ON-state switches***	***Output voltage***
1	2	Sn1, Sn2', Sn3'	$+2V_{dc}$
2	1	Sn1, Sn2',Sn3	$+V_{dc}$
3	0	Sn1, Sn2, Sn3'	0
4	0	Sn1',Sn2',Sn3	0
5	-1	Sn1', Sn2, Sn3'	$-V_{dc}$
6	-2	Sn1',Sn2, Sn3	$-2V_{dc}$

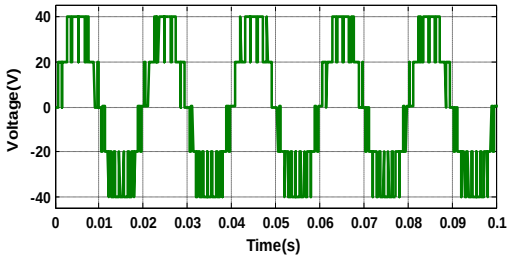

Fig.2 *Five level output voltage waveform of basic module*

Table Irepresents the switching states of a basic module of the proposed structure.As seen from Table I, at any instant only maximum three switches turn on simultaneously. To generate five-level output

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voltage in the conventional CHB MLI, eight switches would be required and four switches turn ON at each instant. Therefore the conduction losses of the proposed MLI are lesser than that of CHB MLI and the quantity of switches is fewer than the traditional CHB MLI, so the switching losses of the proposed inverter will be reduced. The proposed modular MLI is consisting ofseries connection of basic module. Since each module includes two isolated dc sources, so with E number of voltage sources there are (E/2) basic module. The generalized structure of proposed MLI with n basic module that involves E dc sources is depicted in Fig. 3. So, the relationship between E and n can be written as (n=E/2).

Here, proposed MLI with E isolated dc sources is considered. It can be seen from Fig. 3 that there are three switches for each isolated dc source, so the total number of switches can be evaluated as

$$N_{switch} = 3E \quad (1)$$

The total number of output voltage levels can be obtained as follows

$$N_L = 2E + 1 \quad (2)$$

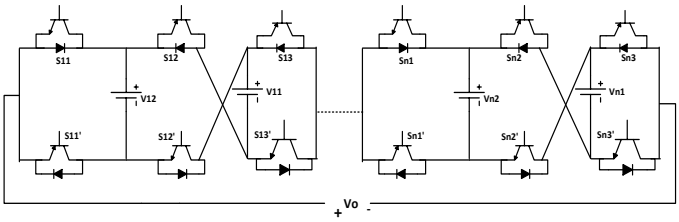

Fig. 3*Generalized structure of proposed modular MLI*

III. MODULATION SCHEME

Several modulation methods have been proposed in the literature for multilevel inverter such as selective harmonic elimination, space vector pulse width modulation (SV-PWM), nearest level control and multicarrier sinusoidal pulse width modulation (SPWM). In this study, voltage balanced based modified pulse width modulation (SPWM) [10] is used for proposed modular MLI. The schematic diagram switching scheme and corresponding signals of the switching scheme aredepicted in Fig. 4. Eight triangular waves of 2-KHz frequency are used as multicarrier signals. Carrier signals are arranged in alternate phase opposition disposition (APOD) SPWM [12-15]. A sinewave of 50-Hz frequency is taken as the modulating signal. A continuous comparison of the reference signal with carrier signals is curried out. Generated signals from the comparator are added so as to obtain combined signal that acquires the same wave shape as that of the desired output voltage level waveform.

The switching signals are obtained from combined signal by comparing with the desired level signal, and are fed to the circuit switches corresponding to the level using look-up table as shown in Table I

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IV. SIMULATION RESULTS

To verify the performance of proposed modular MLI, a single phase nine-level inverter is implemented as shown in Fig. 4.It consists of four isolated DC voltage sources each have 20V magnitude and series R-L AC load. This generates nine-level output voltage waveform of peak amplitude of 80V. The simulation studies have been performed using MATLAB/SIMULINK ver. 7.8 running on a computer (core i7-4770, 3.40 GHz, 2 GB RAM).

Switching states of the proposed nine-level inverter are specified in table II according to the operation using voltage balanced switching control i.e. SPWM. In table II, '1' indicates the switching ON and '0' indicates switching OFF. The output voltage and load current waveforms for different modulation indicesof the 9-level inverter are depicted in Fig. 5, 6 and 7 with harmonic spectrum of the output voltage. It seems quite promising for the partial objective as it is clear from the figures 5, 6 and 7, the total harmonic distortion (THD) is decreasing significantly with the increase in the voltage levels.

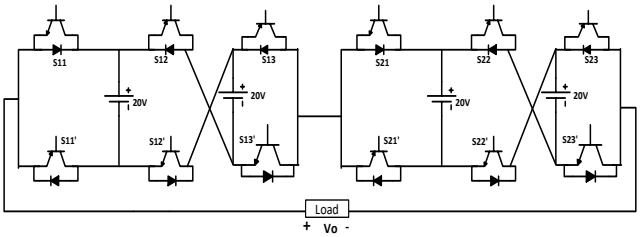
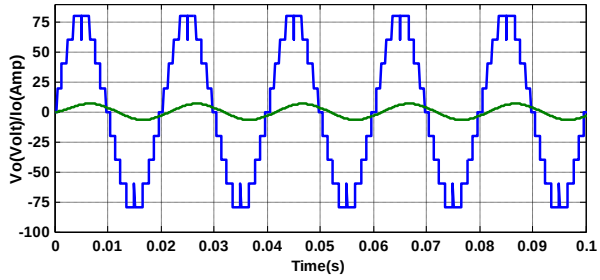


Fig. 4 *Configuration of Nine-level inverter of proposed MLI*



(a). Voltage and current waveforms

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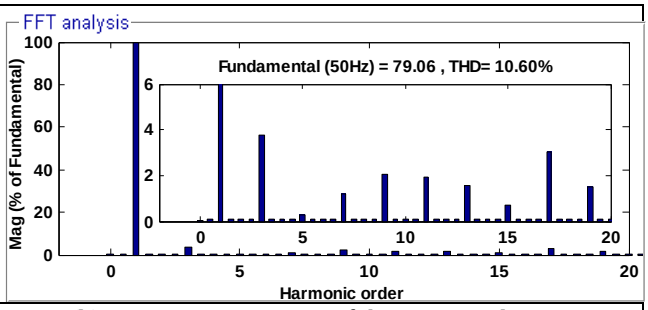

(b). Harmonic spectrum of the output voltage

Fig.5 *for modulation index = 1*

TABLE II. SWITCHING STATE OF 9-LEVEL INVERTER FOR PROPOSED MLI

S.No.	***Switching state***						***Output voltage V_o***
	S_{11}	S_{12}	S_{13}	S_{21}	S_{22}	S_{23}	
1	1	0	0	1	0	0	+80V
2	1	0	0	1	0	1	+60V
3	1	0	0	0	0	1	+40V
4	1	0	1	0	0	1	+20V
5	1	1	0	1	1	0	0
6	0	1	1	0	0	1	- 20V
7	0	1	1	0	0	1	-40V
8	0	1	1	0	1	0	-60V
9	0	1	1	0	1	1	-80V

V. CONCLUSION

The contribution of this paper is to present a modular structure for multilevel inverter. This modular multilevel inverter offers less number of components including power switches and gate driver circuits. The reduction in circuit components results reduction in size of circuit, total cost, and simple switching control scheme. The providedcomparative study shows the superiority of proposed MLI over the conventional CHB MLI on basis of complexity, switches count and THD reduction

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